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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/374,258	08/13/1999	THADDEUS JOHN GABARA	73-1	3509

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EXAMINER	
KUMAR, PANKAJ	
ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/374,258	GABARA ET AL.	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 15-18* is/are rejected.

7)☒ Claim(s) *12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. DETAILED ACTION

Specification

2. The abstract of the disclosure is objected to because it is too long. Abstract must be no more than 150 words. Correction is required. See MPEP § 608.01(b).

3. Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

5. A person shall be entitled to a patent unless –

6. (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1-11, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ho USPN 6418176.

9. As per claim 1, Ho teaches an apparatus comprising:

10. first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal (Ho fig. 5: 92, 94, 96), the processing circuits performing the sampling function utilizing at least one clock signal (Ho paragraph 19; fig. 6);

11. a logic circuit coupled to outputs of each of the first, second and third processing circuits (Ho fig. 5: 100, 102), and operative to generate a control signal indicative of the presence or absence of a desired relationship between the at least one clock signal and the first, second and third versions of the given signal; and

12. a selection circuit having an input coupled to an output of the logic circuit (Ho fig. 5: 70, 72), wherein the selection circuit is responsive to the control signal to alter a relationship between the at least one clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship (Ho paragraph 19: "The control circuit 86 operates the output multiplexers 70,72,74,76 such that the data is read from the FIFO circuit 66,68, and provided to the output flip-flops 78,80,82,84 in two consecutive cycles of the recovery clock signal.").

13. As per claim 2, Ho teaches the apparatus of claim 1 wherein the desired relationship comprises a desired voltage amplitude relationship (Ho fig. 6: internal clock has an amplitude).

14. As per claim 3, Ho teaches the apparatus of claim 1 wherein the desired relationship comprises a desired frequency relationship (Ho fig. 6: internal clock has an frequency).

15. As per claim 4, Ho teaches the apparatus of claim 1 wherein the desired relationship comprises a desired phase relationship (Ho fig. 6: internal clock has an phase).

16. As per claim 5, Ho teaches the apparatus of claim 1 wherein the given signal comprises a receive data clock delivered from a deserializer circuit, and wherein the receive data clock is to be synchronized to the at least one clock signal (Ho col. 1 1st paragraph: "Clock forwarding involves sending more than one bit of data through each conductor of a data path in a single cycle of a clock signal"; col. 1 2nd paragraph: "Clock forwarding is useful in situations where the number of data path conductors is limited. For example, the specifications for an integrated circuit (IC) chip set may limit the number of data path pins that are available on certain ICs. In such a situation, the IC designers may include forwarded clock circuitry within particular ICs to allow those ICs to transfer multiple bits through each of their data path pins during a single clock cycle. Such an arrangement may reduce the effect of, or even eliminate, any data transfer bottleneck caused by the limited availability of data path pins.").

17. As per claim 6, Ho teaches the apparatus of claim 1 wherein the at least one clock signal comprises a clock signal associated with a first chip (Ho fig. 6: internal clock), and the given signal comprises a receive data clock synchronous with another clock signal associated with a second chip (Ho fig. 3: 42 forwarded clock signal).

18. As per claim 7, Ho teaches the apparatus of claim 1 wherein the first, second and third versions of the given signal comprise an early version, a middle version and a late version of the

given signal, wherein the middle version corresponds to the early version delayed by a first amount of time, and the late version corresponds to the middle version delayed by a second amount of time (Ho fig. 5: outputs of 92, 94, 96, 98).

19. As per claim 8, Ho teaches the apparatus of claim 7 wherein the first and second amounts of time are substantially the same, such that the middle version of the given signal has a transition edge which is located approximately midway between a corresponding transition edge in the early and late versions (Ho fig. 5: outputs of 92, 94, 96, 98).

20. As per claim 9, Ho teaches the apparatus of claim 1 wherein the first, second and third versions of the given signal are generated by clocking each of at least a subset of the first, second and third versions with a different delayed version of either the at least one clock signal or another clock signal which is synchronous with the at least one clock signal (Ho Col. 1 3rd paragraph "The information signals contain data synchronously with edges of the forwarded clock signals.").

21. As per claim 10, Ho teaches the apparatus of claim 1 wherein each of the first, second and third processing circuits comprises a series-connected set of flip-flops, with each of the flip-flops in the series connection of flip-flops clocked by the clock signal, and wherein the sampling function in each of the first, second and third processing circuits comprises clocking the respective first, second and third versions of the given signal through the corresponding series-connected set of flip-flops (Ho fig. 5: 92, 94, 96, 98).

22. As per claim 11, Ho teaches the apparatus of claim 10 wherein the logic circuit receives an output signal from each of the series-connected sets of flip-flops, and generates the control signal based on whether or not the output signals have the same logic value within a designated sample window (Ho fig. 5: 66, 68).

23. As per claim 15, Ho teaches an apparatus comprising:

24. a first chip (Ho prior to fig. 3 since clock signal 42 has been forwarded) having a first signal associated therewith;

25. a second chip having a second signal (Ho fig. 3: CLK) associated therewith, wherein the first and second signals are asynchronous;

26. a serializer circuit associated with the first chip (not in Ho but in Huscroft fig. 1: 37: combine Ho in view of Huscroft since Ho has parallel data which saves bandwidth, Huscroft first has serial data which it then converts to parallel data);

27. a deserializer circuit (Ho fig. 3) associated with second chip and having an input coupled to an output of the serializer circuit via an interconnect; and

28. (remainder discussed above with respect to other claims) a synchronizer circuit associated with the second chip and having an input coupled to an output of the deserializer circuit, the synchronizer circuit comprising:

29. first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of an output of the

deserializer synchronous with the first signal, the processing circuits performing the sampling function utilizing at least the second signal;

30. a logic circuit coupled to outputs of each of the first, second and third processing circuits, and operative to generate a control signal indicative of the presence or absence of a desired phase relationship between the second signal and the first, second and third versions of the deserializer output; and

31. a selection circuit having an input coupled to an output of the logic circuit, wherein the selection circuit is responsive to the control signal to alter a phase relationship between the second signal and the first, second and third versions of the deserializer output if the control signal indicates the absence of the desired phase relationship.

32. As per claim 16, Ho teaches a method of processing signals, the method comprising the steps of performing a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, utilizing at least one clock signal (Ho fig. 5: 92, 94, 96, 98); generating a control signal indicative of the presence or absence of a desired relationship between the at least one clock signal and the first, second and third versions of the given signal (Ho fig. 5: 100, 102); and altering a relationship between the at least one clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship (Ho paragraph 19: "The control circuit 86 operates the output multiplexers 70,72,74,76 such that the data is read from the FIFO circuit 66,68, and provided to the output flip-flops 78,80,82,84 in two consecutive cycles of the recovery clock signal.").

33. Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kohli USPN 6249542.

34. As per claim 17, Kohli teaches an apparatus comprising:

35. first, second and third processing circuits (Kohli figs. 3, 4), each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, the processing circuits performing the sampling function utilizing a second signal to which the given signal is to be synchronized (Kohli paragraph 37 col. 11 4th paragraph: "During tracking, the copy of the code produced by code generator 76 and applied to exclusive OR correlators 74 by delay 78 is synchronized with the code in satellite signals 72 ... "; col. 12 5th and 6th paragraphs); and a feedback control circuit (Kohli fig. 2 signal goes from.48 to 50 and 66 and then to 68, 70 and then back to 48) having an input coupled to outputs of each of the first, second and third processing circuits (Kohli figs. 3, 4 whose output goes to 46 in fig. 2 which eventually goes to 48), and operative: (i) to generate a control signal indicative of the presence or absence of a desired phase relationship between the second signal and the first, second and third versions of the given signal (Kohli fig. 2: output of 70), and (ii) to alter a phase relationship between the at least one clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired phase relationship (Kohli paragraph 22 indicates that position is reset when a car turns. When a car turns, signal phase will change.).

36. As per claim 18, Kohli teaches an apparatus comprising:

37. first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, the processing circuits performing the sampling function utilizing a second signal to which the given signal is to be synchronized; and a feedback control circuit having an input coupled to outputs of each of the first, second and third processing circuits (up to here discussed above), wherein the feedback control circuit is operative to maintain a desired relationship (Kohli fig. 2: maintaining location information) between the second signal and the first, second and third versions of the given signal based on sample values generated at the outputs of the first, second and third processing circuits (Kohli fig. 2: SAT processor, in conjunction with NAV Soln, maintain a desired relationship between the SAT trackers so that one tracker does not skew far from other trackers).

38. Allowable Subject Matter

39. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

40. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with the underlined portions:

41. As per claim 12, Ho teaches the apparatus of claim 1 wherein the logic circuit comprises a decision logic block for determining the presence or absence of the desired relationship, and a

counter circuit which is incremented or decremented when the decision logic block determines that the desired relationship is absent (not in Ho), and wherein the control signal corresponds to an output of the counter circuit.

42. As per claim 13, Ho teaches the apparatus of claim 1 wherein the logic circuit comprises a decision logic block for determining the presence or absence of the desired relationship, and a ***latch circuit which is set or reset when the decision logic block determines that the desired relationship is absent*** (not in Ho), and wherein the control signal corresponds to an output of the latch circuit.

43. As per claim 14, Ho teaches the apparatus of claim 1 wherein the logic circuit and the selection circuit form at least a portion of a ***closed loop control system*** (not in Ho) for maintaining the desired relationship between the clock signal and the first, second and third versions of the given signal.

44. Conclusion

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Huscroft et al. USPN 6188692, Nakajima USPN 5309438

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

48. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

49. PK
50. November 14, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 11/15/02